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Customer No.: 31561
Application No.: 10/604,173
Docket No.: 10873-US-PA

AMENDMENTS

Please amend the application as indicated hereafter.

To the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

Claims 1-3 (cancelled)

Claim 4 (currently amended) A display driving circuit, comprising:

a plurality of first driving stages, ~~electrically coupled in serial~~;

a plurality of redundant stages, alternatively disposed between the driving stages and electrically coupled to adjacent driving stages in serial, [[and]] wherein each of the redundant stage having a second driving stage installed with a redundant device in parallel, comprises a conducting path so as to transmit an electric signal from the previous first driving stage to the next first driving stage, ~~wherein the redundant stage and the driving stage are electrically connected in serial, and the redundant stage is the driving stage installed with a redundant device~~; and

a plurality of driving lines, wherein each of the driving lines corresponds to one of the first driving stages or the redundant stages respectively, and each of

the driving line is electrically coupled to an output terminal of a corresponding first driving stage or a corresponding redundant stage.

Claim 5 (cancelled)

Claim 6 (previously presented) The display driving circuit of claim 4, wherein each pair of two adjacent redundant stages further comprises at least one another driving stage electrically coupled therebetween.

Claim 7 (currently amended) The display driving circuit of claim [[5]] 4, wherein the redundant device comprises a plurality of transistors electrically coupled in parallel with transistors in the second driving stage.

Claim 8 (currently amended) The display driving circuit of claim 7, wherein the redundant device is capable of supplying an extra conducting path to transmit an electric signal from the previous first driving stage to the next first driving stage via the current redundant stage while the original conducting path in the corresponding second driving stage of the redundant stage is broken.

Claim 9 (currently amended) The display driving circuit of claim 7, wherein the second driving stage comprises six transistors.

Claim 10 (currently amended) A display driving circuit, comprising:

a plurality of driving stage groups~~, electrically coupled in serial~~, and each of the driving stage groups comprises a plurality of first driving stages electrically coupled in serial;

a plurality of redundant stages, alternatively disposed between the driving stages group and electrically coupled to adjacent driving stages group in serial, wherein[[and]] each of the redundant stage having a second driving stage installed with a redundant device in parallel, comprises a conducting path so as to transmit an electric signal from the previous driving stage group to the next driving stage group~~, wherein the redundant stages and the driving stage groups are electrically connected in serial, and the redundant stage is the driving stage installed with a redundant device~~; and

a plurality of driving lines, wherein each of the driving lines corresponds to one of the first driving stages or the redundant stages respectively, and each of the driving line is electrically coupled to an output terminal of a corresponding first driving stage or a corresponding redundant stage.

Claim 11 (cancelled)

Claim 12 (currently amended) The display driving circuit of claim [[11]]10, wherein the redundant device comprises a plurality of transistors electrically coupled in parallel with transistors in the second driving stage.

Claim 13 (currently amended) The display driving circuit of claim 12, wherein the redundant device is capable of supplying an extra conducting path to transmit an electric signal from the previous first driving stage to the next first driving stage via the current redundant stage while the original conducting path in the corresponding second driving stage of the redundant stage is broken.

Claim 14 (currently amended) The display driving circuit of claim 12, wherein the second driving stage comprises six transistors.

Claim 15 (currently amended) The display driving circuit of claim 10, wherein the driving stage group includes N number of a plurality of first driving stages, and the redundant stage is electrically connected subsequent to the driving stage group.

Claim 16 (new) The display driving circuit of claim 10, wherein the first driving stage comprises:

a first transistor, having a gate electrically coupled to an input terminal, a first source/drain electrode electrically coupled to a power supply and a second source/drain electrode;

a second transistor, having a gate electrically coupled to a first clock terminal, a first source/drain electrode electrically coupled to the gate of the second transistor and a second source/drain electrode electrically coupled to the

second source/drain electrode of the first transistor;

a third transistor, having a gate electrically coupled to the gate of the second transistor, a first source/drain electrode electrically coupled to the input terminal and a second source/drain electrode;

a fourth transistor, having a gate electrically coupled to the second source/drain electrode of the first transistor, a first source/drain electrode electrically coupled to the power supply and a second source/drain electrode electrically coupled to an output terminal;

a fifth transistor, having a gate electrically coupled to the second source/drain electrode of the third transistor, a first source/drain electrode electrically coupled to a second clock terminal and a second source/drain electrode electrically coupled to the output terminal; and

a sixth transistor, having a gate electrically coupled to the gate of the third transistor, a first source/drain electrode electrically coupled to the power supply and a second source/drain electrode electrically coupled to the output terminal.

Claim 17 (new) The display driving circuit of claim 16, wherein the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor and the sixth transistor are NMOS transistors.

Claim 18 (new) The display driving circuit of claim 10, wherein a structure of the second driving stage is the same as a structure of the first driving stage.

Claim 19 (new) The display driving circuit of claim 16, wherein the redundant stage comprises:

a seventh transistor, having a gate electrically coupled to an input terminal, a first source/drain electrode electrically coupled to a power supply and a second source/drain electrode;

an eighth transistor, having a gate electrically coupled to a first clock terminal, a first source/drain electrode electrically coupled to the gate of the eighth transistor and a second source/drain electrode electrically coupled to the second source/drain electrode of the seventh transistor;

a ninth transistor, having a gate electrically coupled to the gate of the eighth transistor, a first source/drain electrode electrically coupled to the input terminal and a second source/drain electrode;

a tenth transistor, having a gate electrically coupled to the second source/drain electrode of the seventh transistor, a first source/drain electrode electrically coupled to the power supply and a second source/drain electrode electrically coupled to an output terminal;

an eleventh transistor, having a gate electrically coupled to the second source/drain electrode of the ninth transistor, a first source/drain electrode electrically coupled to a second clock terminal and a second source/drain electrode electrically coupled to the output terminal;

a twelfth transistor, a gate electrically coupled to the gate of the ninth

transistor, a first source/drain electrode electrically coupled to the power supply and a second source/drain electrode electrically coupled to the output terminal;

a thirteenth transistor, having a gate electrically coupled to the gate of the seventh transistor, a first source/drain electrode electrically coupled to the first source/drain electrode of the seventh transistor and a second source/drain electrode electrically coupled to the second source/drain electrode of the seventh transistor;

a fourteenth transistor, having a gate electrically coupled to the gate of the eighth transistor, a first source/drain electrode electrically coupled to the first source/drain electrode of the eighth transistor and a second source/drain electrode electrically coupled to the second source/drain electrode of the eighth transistor;

a fifteenth transistor, having a gate electrically coupled to the gate of the ninth transistor, a first source/drain electrode electrically coupled to the first source/drain electrode of the ninth transistor and a second source/drain electrode electrically coupled to the second source/drain electrode of the ninth transistor;

a sixteenth transistor, having a gate electrically coupled to the gate of the tenth transistor, a first source/drain electrode electrically coupled to the first source/drain electrode of the tenth transistor, a second source/drain electrode electrically coupled to the second source/drain electrode of the tenth transistor;

a seventeenth transistor, having a gate electrically coupled to the gate of the eleventh transistor, a first source/drain electrode electrically coupled to the first source/drain of the eleventh transistor and a second source/drain electrode

electrically coupled to the second source/drain electrode of the eleventh transistor; and

an eighteenth transistor, having a gate electrically coupled to the gate of the twelfth transistor, a first source/drain electrode electrically coupled to the first source/drain electrode of the twelfth transistor and a second source/drain electrode electrically coupled to the second source/drain electrode of the twelfth transistor.

Claim 20 (new) The display driving circuit of claim 19, wherein the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor, the ninth transistor, the tenth transistor, the eleventh transistor, the twelfth transistor, the thirteenth transistor, the fourteenth transistor, the fifteenth transistor, the sixteenth transistor, the seventeenth transistor and the eighteenth transistor are NMOS transistors.